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ANALYSIS OF FAULTS ON MONOPOLAR HVDC TRANSMISSION LINE

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ABSTRACT

The HVDC transmission lines are used for power transmission over long distances, inevitably passing through the complex terrain and operating under harsh weather conditions. Therefore, HVDC transmission lines are susceptible to the faults. This paper presents the analysis of faults on monopolar HVDC transmission line. The impact of LG fault on ac side, ground fault on the dc side, synchronized ac and dc faults, and unsynchronized ac and dc faults on the voltage, current and performance of the converter is investigated. A test system having monopolar HVDC transmission line connected between two utility networks is modeled in MATLAB/Simulink environment.

KEYWORDS: HVDC Transmission Line, Fault, Rectifier, Inverter, Utility Power Network, Power System Model

1. INTRODUCTION

Power system network consists of transmission and distribution lines used to transfer electrical power from generating stations to load centres [1]. HVDC transmission has advantages, such as longer distance, fast and flexible control, lower losses, and larger power transmission capability. The HVDC transmission line has been increasingly used in modern power systems as an alternative to the ac transmission and effective means for enhancing the stability and economy of the overall power grids [2]. The faults frequently occur on the HVDC transmission lines and which is a major cause of HVDC outages [3]. The perfect protection is very important and necessary to ensure the security and reliability of HVDC transmission lines for which complete knowledge of the fault is required.

The wide study of HVDC faults have been reported in the literature. In [4], authors presented a submarine cable fault detection system for the Hokkaido-Honshu HVDC link. Combining this detection with a current difference detection system which operates for any fault occurring on the HVDC transmission line, the high voltage dc line protection system is composed. To predict the location of dc line fault in a HVDC system, a novel algorithm based on travelling wave natural frequency using 10ms current data from the single end is proposed in [5]. In [6], authors proposed a method for fault locating in HVDC transmission lines which only use voltage signal measured at one of the line terminal. The post fault voltage signal is relatively short time window, is considered and the corresponding fault location is estimated based on the similarity of the captured voltage signal to existing patterns. To study the performance of the distance relay on ac grid with an offshore wind HVDC network, an apparent impedance calculation method which utilizes the bus impedance matrix to calculate the impedances viewed by distance relays during three-phase short circuit faults is proposed in [7]. In [8], authors presented the analysis and control of multilevel modular converter based HVDC transmission system under the three possible single lines to ground fault conditions, with the special focus on the investigation of their different fault characteristics. An HVDC fault location scheme is described in [9], which relies on very precise detection of the time of

arrival of fault created surges at both ends of the line.

This paper presents the study of the analysis of faults on monopolar HVDC transmission line. The impact of LG fault on ac side, ground fault on the dc side, synchronized ac and dc faults, and unsynchronized ac and dc faults on the voltage, current and performance of the converter is investigated.

This paper is divided into four sections. Starting with an introduction in section 1, the section 2 covers the test power system model used for the study of faults on monopolar HVDC transmission line on DC side and AC side of the converter. The simulation results and their discussion are presented in section 3. Finally, the concluding remark is included in the section 4.

2. PROPOSED POWER SYSTEM MODEL

The test system used for the analysis of faults on the monopolar HVDC transmission line is shown in Figure 1. The HVDC transmission line is connected between two utility power systems UT-1 and UT-2. The utility system UT-1 is a 500 kV 60 Hz power network and UT-2 is a 345 kV, 50 Hz power network. The HVDC transmission line is connected to the UT-1 network through rectifier station Rect and to the UT-2 network through inverter station INV. The HVDC transmission line of length 300 kms has resistance 0.015 ohms/kms. The filters F-1 and F-2 are RLC filters of ratings 600 MVA, 60 Hz and 600 MVA, 50 Hz respectively. The input voltage of the rectifier is 200 kV as the 500 kV voltages is converted to the 200 kV with the help of transformer. Similarly the output voltage of inverter station is also 200 kV which is further converted into the 345 kV with the help of a transformer. DCF represents the fault on dc side of the rectifier and ACF represent the fault on the ac side of the inverter.

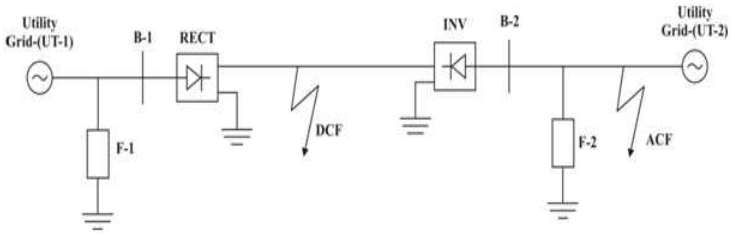

Figure 1: Proposed Model of Power System

3. SIMULATION RESULTS AND DISCUSSIONS

The power system model shown in Figure 1 is simulated in Matlab/Simulink environment. The ac fault is created on the bus B-2 and the dc fault is created on the dc side of the rectifier. The voltage and current measurements are taken at rectifier bus B-1 and inverter bus B-2. The rectifier and inverter stations are switched on at 0.4 seconds and switched off at 1.6 seconds. The simulation is carried out for 2 seconds. The four cases of the study are shown in the subsections follows:

3.1 Single-Line to Ground Fault on AC side

The single line to ground fault on the ac side terminals of the inverter is created at 70 seconds and cleared at the 80 seconds. The three phase voltages and currents measured on the bus B-1 are plotted in the Figure 2 and Figure 3 respectively. The three phase voltages and currents measured on the bus B-2 are plotted in the Figure 4 and Figure 5 respectively. From Figures 2 and 4, it is concluded that the voltage decreases as soon as the rectifier stations are switched on because the rectifier and inverter stations draw the reactive power from the ac side network. Effect is more on rectifier side as compared to the inverter side. During the time for which the fault persist the current in the HVDC transmission line

decreases. The effect of fault on the inverter side converter is minimum.

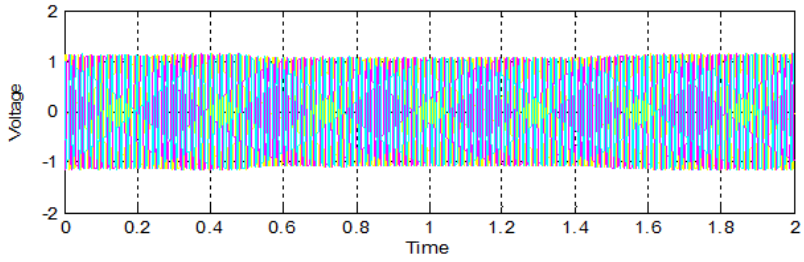

Figure 2: Three Phase Voltage on Rectifier Bus

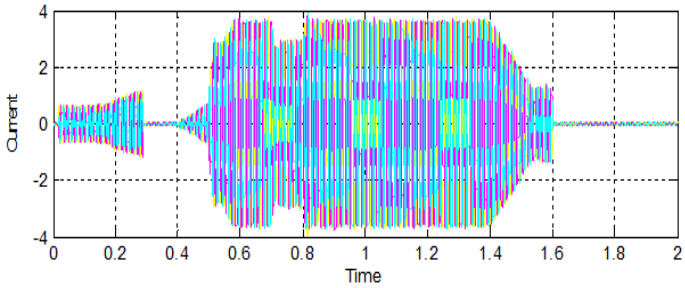

Figure 3: Three Phase Current on Rectifier Bus

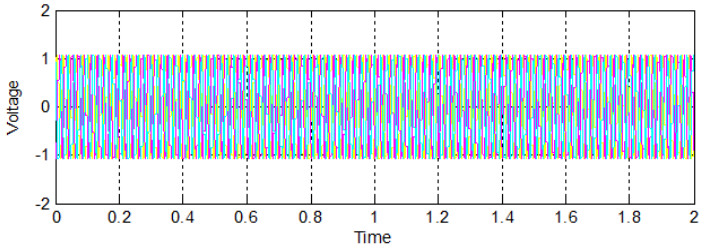

Figure 4: Three Phase Voltage on Inverter Bus

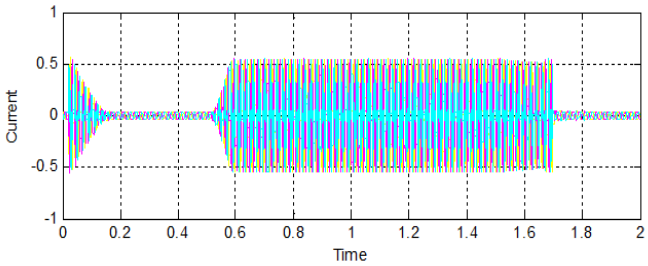

Figure 5: Three Phase Current on Inverter Bus

3.2 Fault on HVDC Line

The line to ground fault is created on the dc side terminals of the rectifier at 70 seconds and cleared at the 75 seconds. The three phase voltages and currents measured on the bus B-1 are plotted in the Figure 6 and Figure 7 respectively. The three phase voltages and currents measured on the bus B-2 are plotted in the Figure 8 and Figure 9 respectively. From the Figures 7 and 9, it is concluded that transients are observed in the current on rectifier side and the current on the inverter side become unstable due to the fault. From the Figures 6 and 8 it is observed that the voltages on rectifier side decreases and effect on the inverter side voltage is minimum.

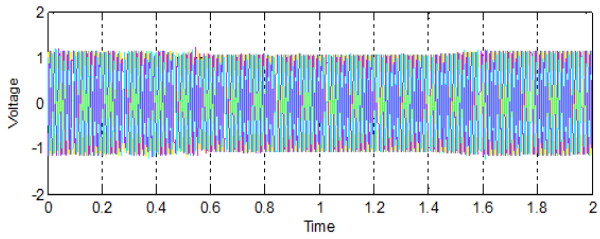

Figure 6: Three Phase Voltage on Rectifier Bus

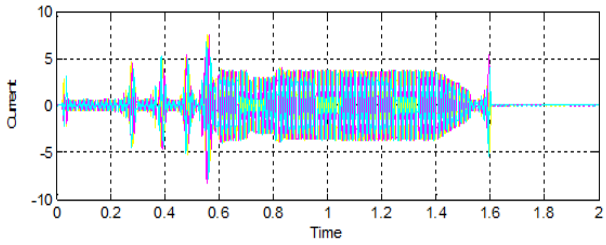

Figure 7: Three Phase Current on Rectifier Bus

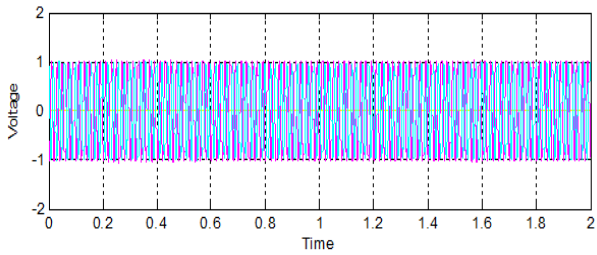

Figure 8: Three Phase Voltage on Inverter Bus

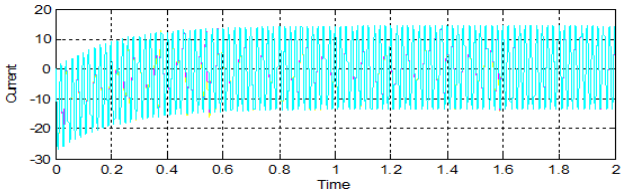

Figure 9: Three Phase Current on Inverter Bus

3.3 Fault on AC and HVDC Lines with same time of Fault Occurrence and Clearance

The single line to ground fault on the ac side terminals of the inverter is created at 70 seconds and cleared at the 80 seconds simultaneously the fault is created on the dc side terminals of the rectifier at 70 seconds and cleared at 80 seconds. The three phase voltages and currents measured on the bus B-1 are plotted in the Figure 10 and Figure 11 respectively. The three phase voltages and currents measured on the bus B-2 are plotted in the Figure 12 and Figure 13 respectively. From Figures 10 and 12, it is concluded that the voltage decreases as soon as the rectifier stations are switched on because the rectifier and inverter stations draw the reactive power from the ac side network the effect is pronounced as compared to the ac of dc faults. Effect is more on rectifier side as compared to the inverter side. During the time for which the fault persist the current in the HVDC transmission line decreases which is high as compared to the either ac or dc fault. After the clearance of the faults the transients and oscillations are observed in the currents as depicted in the Figures 11 and 13. The effect of fault on the inverter side converter is minimum.

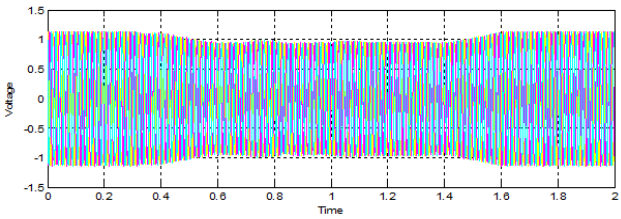

Figure 10: Three Phase Voltage on Rectifier Bus

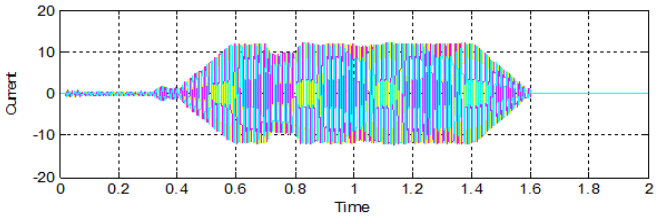

Figure 11: Three Phase Current on Rectifier Bus

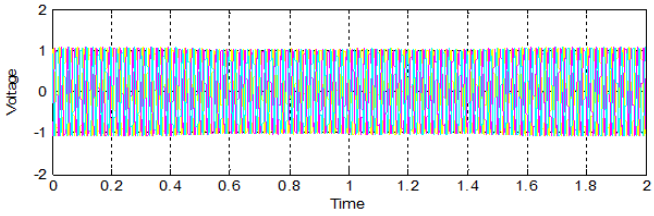

Figure 12: Three Phase Voltage on Inverter Bus

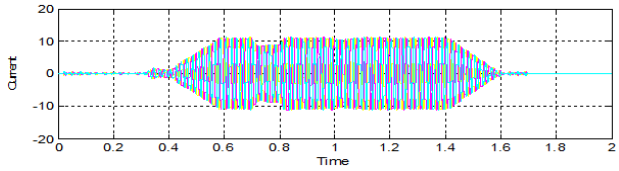

Figure 13: Three Phase Current on Inverter Bus

3.4 Fault on AC and HVDC Lines with Different Time of Fault Occurrence and Clearance

The single line to ground fault on the ac side terminals of the inverter is created at 70 seconds and cleared at the 80 seconds simultaneously the fault is created on the dc side terminals of the rectifier at 70 seconds and cleared at 75 seconds. The three phase voltages and currents measured on the bus B-1 are plotted in the Figure 14 and Figure 15 respectively. The three phase voltages and currents measured on the bus B-2 are plotted in the Figure 16 and Figure 17 respectively. From Figure 14 and 16, it is concluded that the voltage decreases as soon as the rectifier stations are switched on because the rectifier and inverter stations draw the reactive power from the ac side network the effect is pronounced as compared to the ac of dc faults. Effect is more on rectifier side as compared to the inverter side. During the time for which the fault persist the current in the HVDC transmission line decreases which is high as compared to the either ac or dc fault. After the clearance of the faults the transients and oscillations are observed in the currents as depicted in the Figures 15 and 17. The effect of fault on the inverter side converter is minimum.

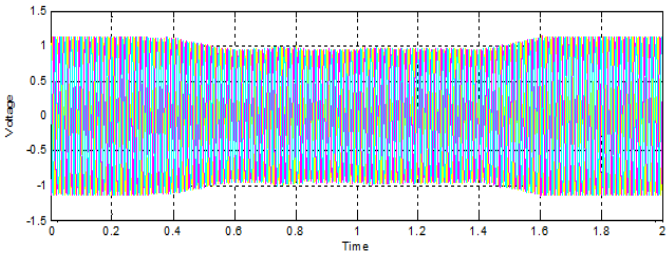

Figure 14: Three Phase Voltage on Rectifier Bus

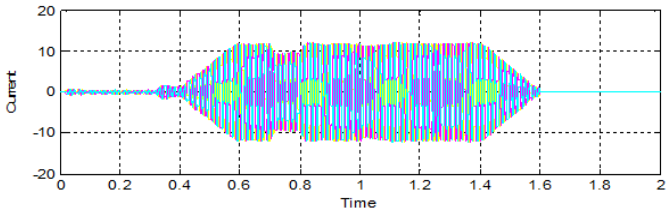

Figure 15: Three Phase Current on Rectifier Bus

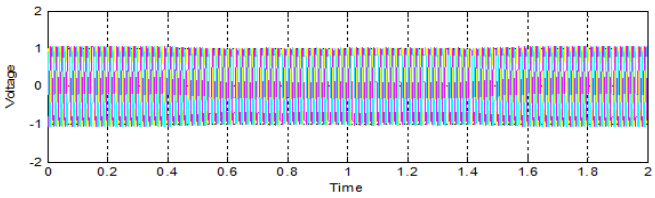

Figure 16: Three Phase Voltage on Inverter Bus

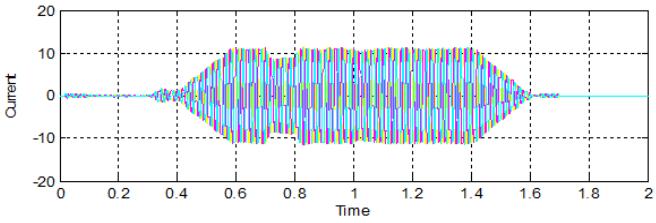

Figure 17: Three Phase Current on Inverter Bus

4. CONCLUSIONS

In this paper, the analysis of ac and dc faults on the monopolar HVDC transmission line is carried out. The analysis is carried out for the impact of LG fault on ac side, ground fault on the dc side, synchronized ac and dc faults, and unsynchronized ac and dc faults is carried out. The effect of simultaneous ac and dc faults is maximum which results in transients and oscillations in the current after clearance of the fault. During the faulty conditions the current decreases from its normal value. Faults also affect the performance of the converter stations. The voltages are changes during the faulty conditions. The effect is maximum on the rectifier station as compared to the inverter station.

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APPENDICES

BIOGRAPHIES

Naveen Gaur received Engineering Diploma, from **Govt**. polytechnic college, Ajmer, India in 2000. He received B.E. Electrical from Rajasthan Institute of Engg. And Tech. Jaipur, India in 2004 and M. Tech. (Power System) from Bhagwant University, Ajmer, India, in 2014

Presently he is working as a Principal at Aryan Polytechnic College, Ajmer, India. He also **w**orked as a Principal at Santosh Adarsh Pvt. ITI, Riya Badi, Nagaur, since July-2013 to Aug-14 and also worked as a Lecturer at Aryan Polytechnic College, Ajmer from Oct-2011 to July-2013. His research interest includes the power system and power electronics. He is author of 3 international journal research papers.

Ram Niwash Mahia received his B.E. degree in Electronics instrumentation and Control Engineering from Govt. Engineering College Bikaner, Bikaner, India and his M.E. degree in Control and Instrumentation under Electrical Department from Delhi College of Engineering, Delhi, India in 2007 and 2009, respectively. He is pursuing Ph.D. degree in Information Communication and Technology from Indian Institute of Technology Jodhpur, Rajasthan, India, since August-2011. From March 2010 to july-2011, he was an Assistant Professor with the Department of Electronics Instrumentation and Control Engineering, Global Institute of Technology, Jaipur, Rajasthan, India. His research interests include control of multi-agent systems, nonlinear control, robust control and its applications for uncertain systems.

Om Prakash Mahela was born in Sabalpura (Kuchaman City) in the Rajasthan state of India, on April 11, 1977. He studied at Govt. College of Engineering and Technology (CTAE), Udaipur, and received the electrical engineering degree from Maharana Pratap University of Agriculture and Technology (MPUAT), Udaipur, India in 2002. He received M. Tech. in 2013. He is currently pursuing PhD from Indian Institute of Technology, Jodhpur, India.

From 2002 to 2004, he was Assistant Professor with the RIET, Jaipur. From 2004 to 2013, he has been Junior Engineer-I with the Rajasthan Rajya Vidhyut Prasaran Nigam Ltd. (RRVPNL), India. Presently he has been Assistant Engineer with RRVPNL. His special fields of interest are Transmission and Distribution (T&D) grid operations, Power Electronics, Power Quality, Renewable energy sources and Load Forecasting. He is an author of 38 International Journals and conference papers. He is a Member of IEEE. He is Member of IEEE Power & Energy Society. Mr. Mahela is recipient of University Rank certificate from MPUAT, Udaipur, India, in 2002 and Gold Medal for M. Tech. in 2013.